Amendments to the Drawings

Kindly substitute the enclosed formal drawing sheet 2/8 for the corresponding drawing sheet originally filed with the application. The attached formal drawing sheet 2/8 includes "Replacement Sheet" label as required under C.F.R. §1.121(d).

Attachments: Replacement sheet 2/8

Annotated sheet showing changes

Remarks

Entry of the amendments, reconsideration of the application, as amended, and allowance of all pending claims are respectfully requested. Claims 1, 3-7, 9-13, 15-19, and 21-24 remain pending.

In the Office Action dated March 10, 2006, the drawings were objected to because the "Replacement Sheet" label was missing; the disclosure was objected to because of informalities; claims 1-2, 4, 7-8, 10, 13-14, 16, 19-20 and 22 were rejected under 35 U.S.C. 102(e) as being unpatentable over Averbuj et al.: and claims 3, 5-6, 11-12, 15, 17-18, 21, and 23-24 were rejected under 35 USC 103(a) over Averbuj et al. and Ilyadis et al. Reconsideration is respectfully requested.

The objections to the drawings and disclosure have been overcome as follows. A new drawing with the "Replacement Sheet" label is filed herewith. The specification has been amended to update the related application information.

Claims 1, 7, 13 and 19, respectively, were amended to incorporate the limitations of cancelled claims 2, 8, 14 and 20, respectively. These claims each now recite: "the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines." The scalability feature is described throughout the specification, e.g., in paragraphs [0033] and [0040], and the command transfer input and output lines are illustrated in the drawing figures 3, 4, and 8, for example. No new matter has been added.

The applicants respectfully traverse the rejections under Section 102 for the following reasons.

Averbuj et al. teaches a built-in self-test architecture having three tiers: a centralized BIST controller, a set of sequencers, and a set of memory interfaces. The BIST controller stores a set of commands that generically define an algorithm for testing memory modules. The sequencers interpret the commands in accordance with a command protocol and generate sequences of memory operations. The memory interfaces apply the memory operations to the memory module in accordance with the physical characteristics of the memory module.

The applicants agree with the Examiner that Averbuj et al. mention hierarchical control. However, the hierarchical control of Averbuj et al. is not scalable. In particular, Averbuj et al. do not teach or suggest "the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines", as recited in the claims, as amended. This is clear from inspection of the drawings of Averbuj et al. For example, in Fig. 1, Averbuj et al. clearly show a multi-dropped, or a "fanout", type structure, i.e., wherein a single line is dropped, or connected to, multiple points. Such a structure is not scalable, in contrast to the applicants' structure, for which each command transfer block in each level of the hierarchical structure has the an equal number of input lines and output lines. This is clear from Figs. 3 and 8 of the present application, which show an equal number of input lines and output lines for each command transfer block in their hierarchical structure, thus advantageously allowing for unlimited scalability, unlike the multi-dropped line structure of Averbuj et al. Thus, while the applicants' structure, as recited in the amended claims, advantageously allows for unlimited scalability in a hierarchical control, Averbuj et al. describes a controlled domain that is predesigned to be hierarchical, and thus would not allow for unlimited scalability.

Claims 1, 7, 13, and 19, particularly as amended, are therefore believed to be patentable over Averbuj et al. under 35 USC 102. Claims 4, 10, 16 and 22, which each recite LBIST, depend from and contain all the limitations of claims 1, 7, 13 and 19, respectively, and are thus likewise believed to be patentable.

The applicants further traverse the rejections under Section 103 on the suggested combination of Averbuj et al. and Ilyadis et al. for the following reasons.

Initially, for the reasons described hereinabove, the applicants' claims, particularly as amended, are distinguishable from Averbuj et al. based in part on the recitation of "the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines. " This particular command transfer structure allows for unlimited scalability, which is not taught or suggested by Averbuj et al., who use a multi-dropped line, or fanout, structure,

which does not allow for unlimited scalability, as the applicants' command transfer structure does. Thus, as described below, even if Ilyadis et al. could be combined with Averbuj et al., then such a combination would still be deficient with respect to this structure, as recited in the amended claims.

The patent to Ilyadis et al. is cited with respect to the synchronization feature. Ilyadis et al. describe a network hub for interconnection of modular devices, with timing synchronization provided by a global synchronization mechanism. Ilyadis et al. specifically describe their global synchronization mechanism in column 4, lines 19-31, as follows:

> In addition to the six lines of the IMB 150, synchronization of data is provided by a single global synchronization mechanism 58. The global synchronization mechanism 58 is shown as having two clock lines labeled 158 and 160. Preferably, global synchronization line 158 should have a clock speed of one half the clock speed of global synchronization line 160. Still more preferable, global synchronization line 158 will run at 10 MHz and global synchronization line 160 will run at 20 MHz. In an alternate embodiment, the global synchronizations 158 and 160 may be replaced by a single global synchronization line, as discussed more fully with reference to FIG. 7.

The applicants respectfully submit that Ilyadis describes a classical type synchronization mechanism and, moreover, do not teach or suggest a communication protocol comprising a global synchronization signal, as recited in claims 3, 9, 15 and 21, which is used in a system for testing integrated circuitry, comprising a scalable command transfer control hierarchy, as recited in the independent claims from which these claims depend. Furthermore, Ilyadis et al. do not teach or suggest the applicants' scalable command transfer control hierarchy in a system for testing integrated circuitry "wherein the command transfer control hierarchy controls the LBIST system such that LBIST testing is performed on the clock domains synchronously," as recited in claims 5, 11, 17 and 23; and similarly in claims 6, 12, 18 and 24.

Even assuming *arguendo* that Ilyadis et al. teach the synchronization feature of the applicants (which the applicants respectfully maintain that they do not), Averbuj et al. do not

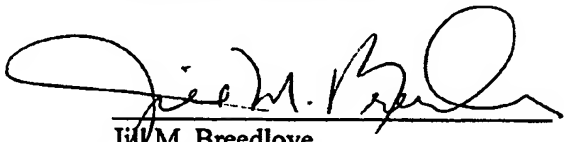
teach or suggest "the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines", as recited in the amended claims and described hereinabove, so that any suggested combination of Averbuj et al. and Ilyadis et al. would still be deficient, and the applicants' invention, as recited in the amended claims, would not be rendered obvious thereby.

Therefore, since neither Averbuj et al. nor Ilyadis et al., alone or in combination, teach or suggest a system for testing integrated circuitry comprising a plurality of clock domains "the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines", as recited in the claims, as amended, the applicants' invention is not rendered obvious thereby.

Reconsideration and allowance of claims 1, 3-7, 9-13, 15-19, and 21-24 are thus respectfully requested.

Should the Examiner wish to discuss this case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,



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Dated: August 4, 2006.

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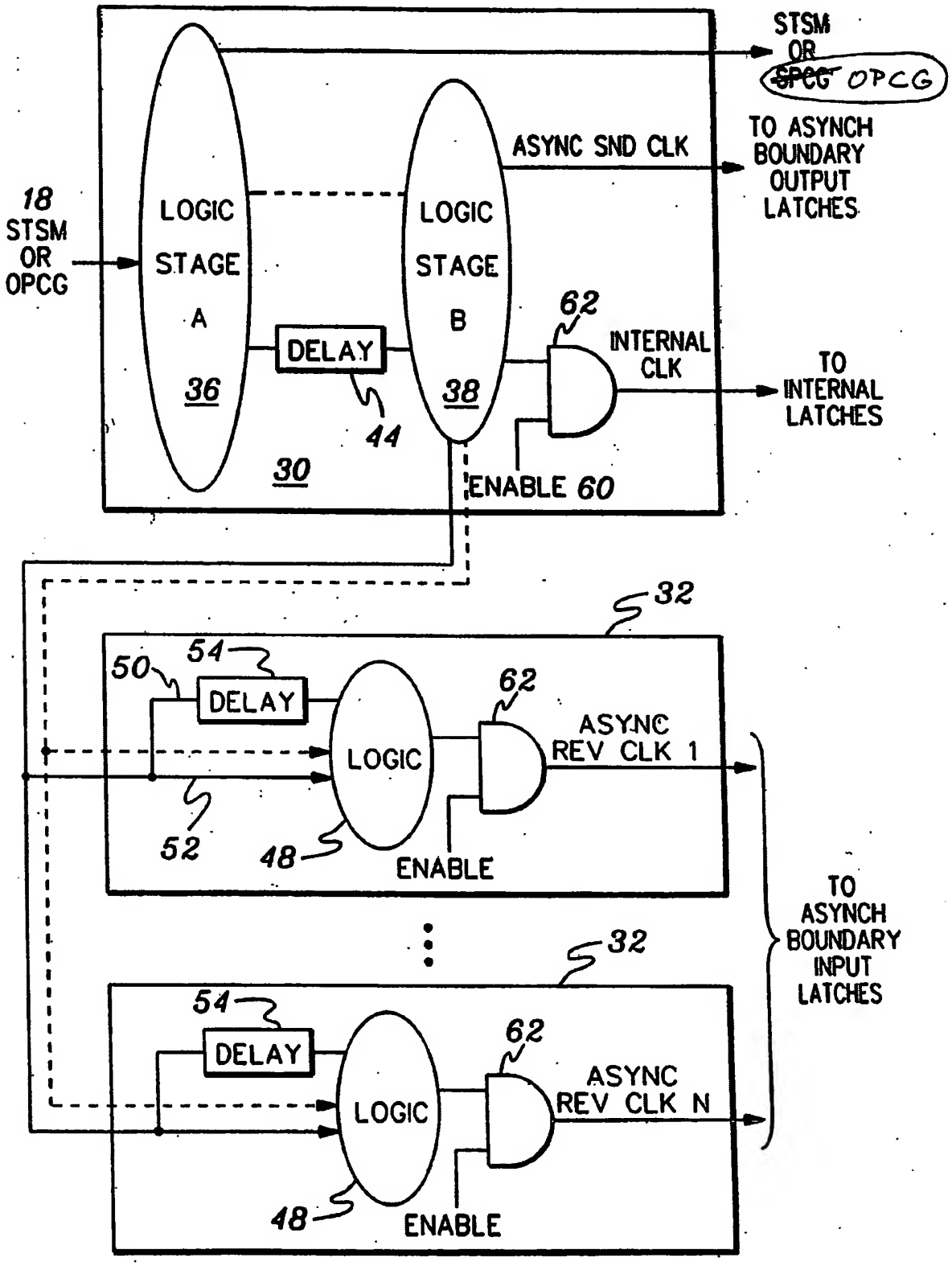
STSM OR OPCG
TO ASYNCH BOUNDARY OUTPUT LATCHES
ASYNC SND CLK
18
STSM OR OPCG
LOGIC STAGE A
36
DELAY
44
LOGIC STAGE B
38
62
INTERNAL CLK
TO INTERNAL LATCHES
30
ENABLE 60
32
50
54
DELAY
LOGIC
62
ASYNC REV CLK 1
52
48
ENABLE
32
54
DELAY
LOGIC
62
ASYNC REV CLK N
48
ENABLE
TO ASYNCH BOUNDARY INPUT LATCHES

fig. 2